

## Claims

1. Multiplier device comprising first to  $n^{\text{th}}$  multipliers  $M_1$  to  $M_n$  for multiplying a carrier modulated information signal with first to  $n^{\text{th}}$  mutually phase shifted and identical, substantially square wave mixing signals  $MS_1$  to  $MS_n$  with 50% duty cycle, characterized by  $n$  being greater than 2, outputs of said multipliers  $M_1$  to  $M_n$  being respectively coupled through weighting circuits  $W_1$  to  $W_n$  with respective fixed weighting factors  $WF_1$  to  $WF_n$  to an adder circuit, said mixing signals  $MS_1$  to  $MS_n$  having respective phase angles  $\varphi_i$  corresponding to  $\varphi_i = i * \Delta\varphi$ , said weighting factors  $WF_i$  corresponding to the sine value of said respective phase angles  $\varphi_i = i * \Delta\varphi$  with  $\Delta\varphi$  being the mutual phase difference between each two phase consecutive mixing signals corresponding to  $\pi/(n + 1)$  and  $i$  varying from 1 to  $n$ .
- 15 2. Multiplier device according to claim 1, characterized by  $n$  corresponding to  $(N+1)/2$  for an elimination of all harmonics up to the  $N^{\text{th}}$  order from the output of said adder circuit.
- 20 3. Multiplier device according to claim 1 or 2, characterized by said mixing signals  $MS_1$  to  $MS_n$  being derived from a local oscillator signal with frequency  $f_0$  through an arrangement of fixed phase shift means and/or frequency divider means.
- 25 4. Multiplier device according to claim 3, characterized by a local oscillator circuit supplying an oscillator signal with frequency  $f_0$  to a serial arrangement of first to  $n^{\text{th}}$  phase shifting means, each providing a fixed phase shift of  $\Delta\varphi$  and supplying respectively mixing signals  $MS_1$  to  $MS_n$  to said first to  $n^{\text{th}}$  multipliers  $M_1$  to  $M_n$ .
- 30 5. Multiplier device according to claim 4, characterized by said local oscillator circuit generating a clock control signal with clock frequency  $n *$

fo being supplied through a frequency divider with dividing factor n to said serial arrangement of first to n<sup>th</sup> phase shifting means, each of said first to n<sup>th</sup> phase shifting means comprising a D-flip-flop being clock controlled by said clock control signal and providing said fixed phase shift of Δφ.